> The disclosure is objected to because of the following informalities: page 7, line 2 change "Fig. 4" to "Figs. 4(a)-(x).
>
> Appropriate correction is required.

The specification has been amended to correct certain informalities pointed out by the Examiner. Specifically, by the present amendment, both the Abstract and the paragraph beginning on page 7, line 2 have been corrected as suggested by the Examiner.

The Examiner has rejected claim 8 under 35 USC §102, as being anticipated by JP 03-129795 ("JP-95") granted to Hitachi Seiko Ltd. The Examiner has stated:

> JP-95 discloses, referring to figure (D) a printed circuit board comprising: an insulative substrate (20); an upper surface pattern (27) and a lower surface pattern (22) provided, respectively, on an upper surface and a lower surface of the insulative substrate; and a blind via hole (28) for electrically connecting the upper surface pattern and the lower surface pattern, wherein an upper portion of the blind via hole is covered by the *lower* surface pattern, the thickness of the upper surface pattern being less than that of the lower surface pattern [claim 8]

The Applicants' respectfully submit that the characterization of JP 03-129795 is incorrect in that the object shown in Figure D of JP 03-129795 is not a "printed circuit board." Instead, it is an element used in forming the printed circuit board. The Applicants' respectfully further submit that the characterization is also incorrect in that the cited element does not show a "lower surface pattern," nor does it show "the thickness of the upper surface pattern being less than that of the *lower* surface pattern."

Referring to Figures 2 (A) through (I) , these show steps used in forming a printed board. Although it is unclear from the drawings the exact nature of the steps, it is apparent that Figure 2 (A) shows a substrate (20) with an upper surface (21) and a lower

surface (22) . Figure 2 (B) shows a blind via hole (25) being formed, and Figure 2 (C) shows that hole being coated so as to electrically connect the upper surface and the lower surface. Figures 2 (D) and 2 (E) apparently show that two of the substrates of Figure 2 (C) are subjected to an etching process, wherein the upper surfaces are etched into two different patterns. Then, in Figure 2 (F) the substrate in Figure 2 (D) is flipped and placed over the substrate in Figure 2 (E), with some type of material (30? or 40?) between the two substrates. Then, in Figure 2 (G), holes (50) and (55) are made the product of Figure 2 (F) . in Figure 2 (H) , the new holes are coated. In the final figure of the series, Figure 2 (1), some sort of pattern is formed in the surface to the top part of this device and the bottom part of the device to produce the printed board. It appears from Figure 2 (I) that the inner surfaces (27) and (37) and outer surfaces (22) and (32) are not etched to the same thickness. It also appears from Figures 2 (D) and 2 (E) that the lower surfaces, (22) and (32) respectively, are not etched, and no pattern is formed in those figures.

None of the figures in Figure 2 (A) through 2 (I) show the present invention, since none of them show "an upper surface pattern and a lower surface pattern" with "the thickness of the upper surface pattern being less than that of the lower surface pattern." Figures 2 (A) through 2 (C) show no surface patterns, since the etching doesn't occur until Figures 2 (D) and (E) . Figures 2 (D) through 2 (E) show only one surface pattern: the one on the upper surface. Figures 2 (F) through 2 (H) show two inner surface patterns, but they are apparently the same size. Figure 2 (1) shows four surface patterns, but they are all apparently the same size.

The feature missing from JP 03-129795 (the thickness of the upper surface pattern being less than that of the lower surface pattern) is an important element of the claimed invention, since when manufacturing such a the printed circuit board, etching for forming the upper surface pattern is facilitated and the lower surface pattern, which defines the bottom of the blind via hole, is not damaged by the laser emission, and the blind via hole is formed in a satisfactory state. (See our specification on page 6, lines 14-20)

Since the cited publication fails to disclose the claimed invention, and since that publication fails to disclose anything about reaching the object taught in the present invention, we respectfully request that the Examiner withdraw his rejection to claim 8.

The Examiner has also rejected claims 1-7 and 9--13 under 35 USC §103 (a) , as being unpatentable over JP 03-129795. The Examiner has stated:

> JP-95 discloses a method for manufacturing a printed circuit board comprising the steps of: coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil; forming an *opening* in the upper surface metal foil at a location corresponding to a blind via hole formation portion of the insulative substrate; forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening; applying a conductor to the blind via hole. JP-95 does not specifically disclose forming an upper surface pattern and a lower surface pattern by respectively etching the upper surf ace metal foil and the lower surface metal foil. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to etch the upper and lower surfaces as is well known in the art to form surface patterns. The motivation for doing so would have been to provide the requisite wiring desired. Additionally, the methods claimed in claims 2-7 and 9-13 are mere obvious variants of the method disclosed in JP-95 and thus would be obvious to one having ordinary skill in the art.

For reasons similar to that discussed above, the Applicants' respectfully submit that the characterizations made about JP 03-129795 are incorrect in regard to this rejection as well.

JP 03-129795 fails to disclose forming an opening in a upper surface metal. foil *(the thickness of which is less than that of the lower surface metal foil)* at a location corresponding to a blind via hole formation portion of the insulative substrate, then forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening [Elements of Claim 1].

According to Figures 2 (A) through 2 (C) , when the blind via hole in JP 03-129795 is formed, the upper surface metal foil is the same thickness as the lower surface metal foil. Therefore, JP 03-129795 not only fails to teach our invention, it furthermore fails to teach a means achieving a primary abject of our invention, as disclosed in our specification on page 2, lines 18-22: "It is an object of the present invention to provide a printed circuit board and method of manufacturing same that facilitate the formation of the upper surface pattern and prevent a laser from damaging the lower metal foil when forming blind via holes."

The importance of having the thickness of the upper surface metal foil less than the thickness of the lower surface metal foil, is discussed in the specification on page 3, lines 11-19, which states; "This facilitates etching of the upper surface pattern, and the thickness of the lower surface metal. foil is such that the lower surface metal foil is prevented from being damaged by the emission of a laser during formation of the blind via hole. Accordingly, the upper pattern is easily formed through etching, damage to the lower surface pattern due to the laser emission is prevented, and a conductor is applied to the blind via hole in a satisfactory state."

Claims 3 through 7 include the limitations of Claim 1 and include further restrictions on how the difference is achieved and the preferred thicknesses for the upper and lower surfaces. None of these further restrictions are taught by JP 03-129795.

Claim 2 differs from Claim 1 in that the upper surface pattern and lower surface pattern are formed before forming a blind via hole. This also is not taught by JP 03-129795.

Instead, the blind via hole in JP 03-129795 is formed when the upper surface metal foil is the same thickness as the lower surface metal foil and before any etching of a surface pattern.

Claims 9 through 13 include the limitations of Claim 2 and include further restrictions on how the difference is achieved and the preferred thicknesses for the upper and lower surfaces. None of these further restrictions are taught by JP 03-129795.

For the above reasons, we respectfully request that the Examiner withdraw his rejection and allow the case to issuance.

Respectfully submitted,

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APPENDIX I - MARKED UP COPY OF AMENDED SPECIFICATION

The paragraph beginning on page 7, line 2:

[Fig. 4 is an explanatory view] Figs. 4(a)-(x) are explanatory views showing a method for manufacturing prior examples of printed circuit boards.

The revised Abstract:

A printed circuit board and a method for manufacturing the same that facilitates the formation of an upper surface pattern and prevents a lower surface metal foil from being damaged when forming a blind via hole with a laser [is provided]. A lower surface and an upper surface of an insulative substrate (5) are respectively coated with a lower surface metal foil (220) and an upper surface metal foil (210), the thickness of which is less than that of the lower surface metal foil (220). Next, an opening (213) is formed in the upper surface metal. foil at a location corresponding to a blind via hole formation portion (35) of the insulative substrate. A blind via hole (3), the bottom of which is the lower surface metal foil, is formed by emitting a laser (8) against the blind via hole formation portion (35) through the opening (213). Then, a metal plating film (23) is applied to the wall of the blind via hole (3), and an upper surface pattern (21) and a lower surface pattern (22) are formed through etching.